UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,442	04/20/2004	Katsuya Arai	60188-841	2727

7590 11/03/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,442	ARAI ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1;5 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *2-4,6-10 and 15-17* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/20/04, 10/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1, 5, and 11-14 in the reply filed on 10/17/2006 is acknowledged.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 5, and 11-14 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5, 13, and 18-20 of copending Application No. 10/913,356. Although the conflicting claims are not identical, they are not patentably distinct from each other. Claim 1 of both applications are exact same except for claim 1 of the

application [10/913,356] recites that the inter-power supply electrostatic discharge protection circuit comprises a first substrate potential control circuit capable of controlling a substrate voltage of the gate insulating element, instead of a first gate voltage control circuit capable of controlling the gate voltage of the gate insulating element as recited in the application [10/827,442]. However, it would have been obvious to those skilled in the art at the time the invention was made to provide the protection circuit without the first substrate potential control circuit as claimed to provide a simpler circuit which does not require the same level of ESD protections.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al., Patent No. 6,920,026.

With respect to claim 1, Chen teaches a semiconductor integrated circuit device [Fig. 8] comprising an external connection terminal [Fig. 8, 120]; an electrostatic discharge protection circuit [Fig. 8, consists of Mp51, Mn51] connected to the external connection terminal; a power supply line [Fig. 8, VDD] connected to the electrostatic discharge protection circuit; a ground line [Fig. 8, VSS] connected to the electrostatic discharge protection circuit; and an inter-power supply electrostatic discharge protection circuit [Fig. 8, 15]] that is connected to the power supply line [Fig. 8, VDD] and the ground line [Fig. 8, VSS], and has a gate insulating element [Fig. 8, transistor Mn8], wherein the inter-power supply electrostatic discharge protection circuit comprises a first gate voltage circuit [Fig. 8, consists of capacitor C6 and resistor R7] capable of controlling the gate voltage of the gate insulating element [Fig. 8, transistor Mn8] as disclosed in Col. 12, lines 31 – Col. 13, lines 20].

With respect to claim 14, Chen teaches that the device further comprises an internal circuit [Fig. 8, 1, internal circuit] connected to the external connection terminal [Fig. 8, 120].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Patent No. 6,920,026, in view of Wu et al., Patent No. 6,552,886.

With respect to claim 5, Chen teaches that the gate-insulating element is a first NMOS transistor [Fig. 8, Mn8] whose source is connected to the ground line [Fig. 8, VSS] and whose drain is connected to the power supply line [Fig. 8, VDD], but does not disclose that the gate-insulating element is a first NMIS transistor, and that the first gate voltage control circuit comprises a first Schmidt trigger circuit. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the NMIS transistor with NMOS transistor for the benefit of having the circuit in a simple structure which would have a small number of manufacturing steps, resulting in a less cost.

Wu teaches an ESD protection circuit. Wu teaches that a first gate voltage circuit comprises a first Schmidt trigger circuit [Fig. 4, consists of inverters 32, 34, 36 and transistor 28] connected at its output to the gate of the first NMOS transistor [Fig. 4, 30], a resistor [Fig. 4, 24] whose one end is connected to the power supply line [Fig. 4, VCC] and whose other end is connected to an input of the first Schmidt trigger circuit; and a capacitor [Fig. 4, 27] whose one end is connected to the ground line [Fig. 4, VSS] and whose other end is connected to the input of the first Schmidt trigger circuit.

Both teachings are analogous electrostatic discharge protection circuits coupled between power and ground. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to combine the teachings of Wu, which teaches a Schmidt trigger circuit, with the ESD circuit of Chen, for the benefit of providing nose immunity at power-up.

With respect to claim 11, Chen teaches that the device comprises an input buffer circuit [Fig. 11, Pre-buffer] connected to the external connection terminal [Fig. 11, 140].

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of Ker et al., Patent No. 6,437,407.

Chen teaches a semiconductor integrated circuit device, but does not disclose that the device further comprises an output circuit and an output pre-buffer circuit.

Ker teaches an ESD circuit for integrated circuits. With respect to claim 12, Ker teaches that the integrated circuit further comprises an output circuit [Fig. 7, consists of transistors 704 and 704'] connected to the external connection terminal [Fig. 7, 702]; and an output pre-buffer circuit [Fig. 7, consists of transistors 708, 710, 708', 710'] connected to the output circuit.

Both teachings are analogous electrostatic discharge protection circuits for integrated circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker, which teaches an output circuit and an output pre-buffer circuit, with the ESD circuit of Chen, because the ESD clamp device is disposed on an output buffer in order to clamp the ESD overstress voltage across the gate oxide during an ESD event.

With respect to claim 13, Ker teaches that the output pre-buffer circuit comprises a first pre-buffer circuit [Fig. 7, consists of transistors 708 and 710] having at its last stage a first pre-buffer connected to the power supply line [Fig. 7, VDD], and a second pre-buffer circuit [Fig. 7, consists of transistors 708' and 710'] having at its last stage a second pre-buffer connected to the power supply line [Fig. 7, VDD], and wherein the output circuit comprises a second PMOS transistor [Fig. 7, 704] whose source is connected to the power supply line [Fig. 7, VDD], whose drain is connected to the external connection terminal [Fig. 7, 702], whose gate is connected to an output terminal of the first pre-buffer, and whose n-type substrate region [Fig. 7, substrate terminal of PMOS transistor 704] is connected to the power supply line [Fig. 7, VDD]; and a second NMOS transistor [Fig. 7, 704'; The PMOS transistor 704' can be replaced by an NMOS transistor, because the drains and sources are fully interchangeable in MOSFETS].whose source is connected to the ground line [Fig. 7, VSS], whose drain is connected to the external connection terminal [Fig. 7, 702], whose gate is connected to an output terminal of the second pre-buffer and whose p-type substrate region [Fig. 7, substrate terminal of NMOS transistor 704'] is connected to the ground line [Fig. 7, VSS].

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
10/30/2006

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800